DATA SHEET

TDA8786; TDA8786A
10-bit analog-to-digital interface for CCD cameras

Product specification
Supersedes data of 1997 May 20
File under Integrated Circuits, IC02

1997 Nov 17

Philips
Semiconductors

PHILIPS

10-bit analog-to-digital interface for CCD cameras

TDA8786; TDA8786A

FEATURES

- Correlated Double Sampling (CDS), AGC, soft clipper, pre-blanking, 10-bit ADC and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- AGC gain from 3.5 to 33.5 dB (in 0.1 dB steps)
- Programmable soft clipper for white compression (starting at 40% of the input signal)
- Standby mode available for each block for power saving applications (19 mW)
- 6 dB fixed gain analog output for analog iris control
- 8-bit and 10-bit DAC included for analog settings
- Low power consumption of only 475 mW (typ.)
- 5 V operation and 2.5 to 5 V operation for the digital outputs
- CDS control pulse: TDA8786 = HIGH; TDA8786A = LOW
- TTL compatible inputs, TTL and CMOS compatible outputs.

GENERAL DESCRIPTION

The TDA8786; TDA8786A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, AGC, a soft clipper circuit and a low power 10-bit Analog-to-Digital Converter (ADC) together with its reference voltage regulator.

The AGC and soft clipper circuits are controlled by on-chip DACs via a serial interface.

A 10-bit DAC controls the ADC input clamp level.

A pre-blanking function is also included.

An additional DAC is provided for additional system controls; its output voltage range is 1.4 V (p-p) which is available at pin OFDOUT.

APPLICATIONS

- CCD camera systems.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	83	–	mA
I_{CCD}	digital supply current		–	16	–	mA
I_{CCO}	digital outputs supply current	f_{CLK} = 18 MHz; C_L = 20 pF; ramp input	–	1	–	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	CDS input voltage (peak-to-peak value)		–	400	1200	mV
G_{CDS}	CDS output amplifier gain		–	6	–	dB
$f_{CLK(max)}$	maximum clock frequency		18	–	–	MHz
AGC_{dyn}	AGC dynamic range		–	30	–	dB
$N_{tot(rms)}$	total noise from CDS input to ADC output (RMS value)	gain = 3.5 dB	–	0.5	–	LSB
P_{tot}	total power consumption		–	475	–	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8786G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
TDA8786AG			

BLOCK DIAGRAM

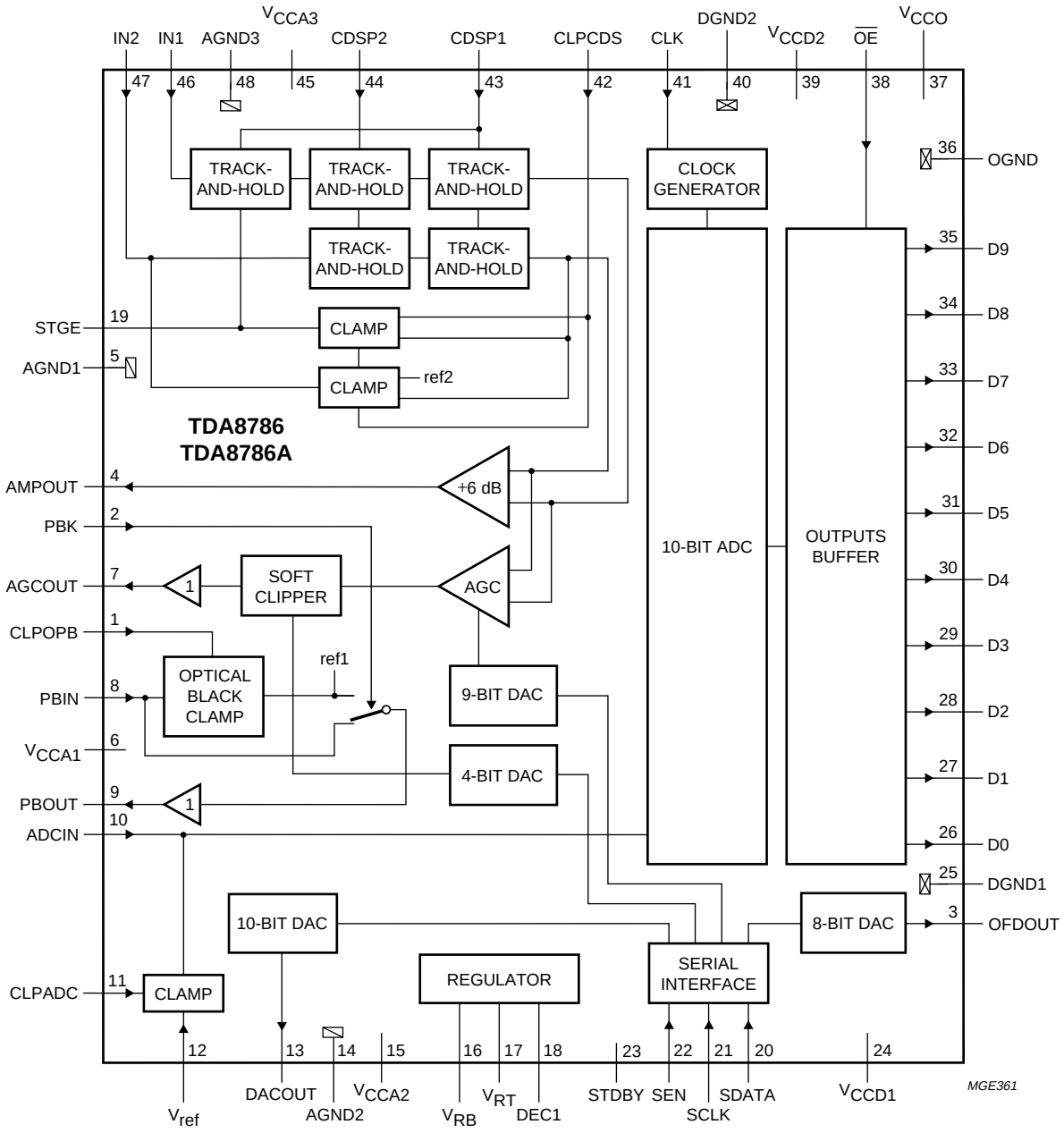


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
CLPOPB	1	optical black clamp control pulse input (active HIGH for TDA8786, active LOW for TDA8786A)
PBK	2	pre-blanking control pulse input; if PBK is HIGH (LOW) the signal is replaced by the optical black level for TDA8786 (TDA8786A)
OFDOUT	3	analog output of the additional 8-bit control DAC (controlled via the serial interface)
AMPOUT	4	CDS amplifier output (fixed gain = +6 dB)
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
AGCOUT	7	AGC and soft clipper amplifier signal output
PBIN	8	optical black clamp and pre-blanking block signal input (from AGCOUT via a capacitor)
PBOUT	9	optical black clamp and pre-blanking block signal output
ADCIN	10	ADC analog signal input (from PBOUT or AGCOUT via a capacitor)
CLPADC	11	clamp control input for ADC analog input signal clamp (active HIGH for TDA8786 and active LOW for TDA8786A)
V_{ref}	12	ADC input clamp reference voltage (normally connected to pin VRB or DACOUT)
DACOUT	13	DAC output for ADC clamp level
AGND2	14	analog ground 2
V_{CCA2}	15	analog supply voltage 2
V_{RB}	16	ADC reference voltage (BOTTOM) code 0
V_{RT}	17	ADC reference voltage (TOP) code 1023
DEC1	18	decoupling 1 (decoupled to ground via a capacitor)
STGE	19	CDS offset storage
SDATA	20	serial data input for the 4 control DACs (9-bit DAC for AGC gain, 4-bit DAC for soft clipper; additional 8-bit DAC for OFD output voltage; 10-bit DAC for ADC clamp level and the stand-by mode per block; see Table 1)
SCLK	21	serial clock input for the control DACs and their serial interface; see Table 1
SEN	22	enable input for the serial interface shift register (active when SEN = logic 0); see Table 1
STDBY	23	stand-by control pin (active HIGH); all the output bits are logic 0 when stand-by is enabled
V_{CCD1}	24	digital supply voltage 1
DGND1	25	digital ground 1
D0	26	ADC digital output 0 (LSB)
D1	27	ADC digital output 1
D2	28	ADC digital output 2
D3	29	ADC digital output 3
D4	30	ADC digital output 4
D5	31	ADC digital output 5
D6	32	ADC digital output 6
D7	33	ADC digital output 7
D8	34	ADC digital output 8
D9	35	ADC digital output 9 (MSB)
OGND	36	digital output ground

SYMBOL	PIN	DESCRIPTION
V_{CCO}	37	digital output supply voltage
$\overline{OE}$	38	output enable (LOW: digital outputs active; HIGH: digital outputs high impedance)
V_{CCD2}	39	digital supply voltage 2
DGND2	40	digital ground 2
CLK	41	ADC clock input
CLPCDS	42	CDS clamp control input (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP1	43	CDS control pulse input 1 (active HIGH for TDA8786; active LOW for TDA8786A)
CDSP2	44	CDS control pulse input 2 (active HIGH for TDA8786; active LOW for TDA8786A)
V_{CCA3}	45	analog supply voltage 3
IN1	46	input signal 1 from CCD (usually black channel)
IN2	47	input signal 2 from CCD (usually video channel)
AGND3	48	analog ground 3

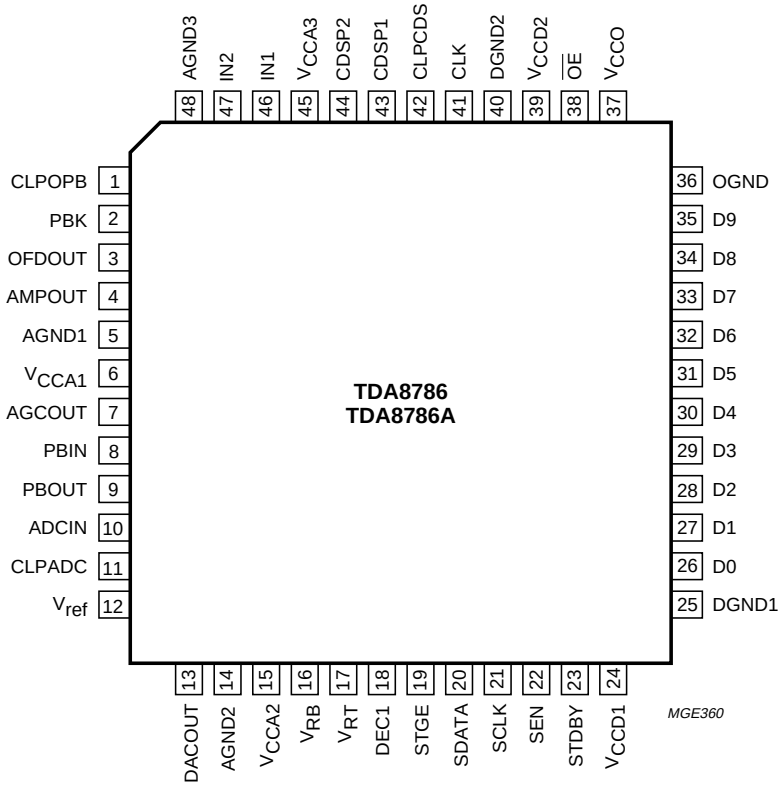


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+7.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		–1.0	+1.0	V
	between V_{CCA} and V_{CCO}		–1.0	+4.0	V
	between V_{CCD} and V_{CCO}		–1.0	+4.0	V
V_i	input voltage	referenced to V_{SSA}	–0.3	+7.0	V
$V_{CLK(p-p)}$	AC input voltage for switching (peak-to peak-value)	referenced to V_{SSD}	–	V_{CCD}	V
I_o	output current		–	10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	operating ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +7.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

CHARACTERISTICS

V_{CCA} = V_{CCD} = 4.75 V; V_{CCO} = 2.6 V; f_{CLK} = 18 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	4.75	5.5	V
V_{CCD}	digital supply voltage		4.5	4.75	5.5	V
V_{CCO}	digital outputs supply voltage		2.5	2.6	5.5	V
I_{CCA}	analog supply current		–	83	–	mA
I_{CCD}	digital supply current		–	16	–	mA
I_{CCO}	digital outputs supply current	C_L = 20 pF on all data outputs; ramp input	–	1	–	mA
Digital inputs						
CLOCK INPUT: CLK (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{CLK} = 0.8 V	–1	–	+1	μA
I_{IH}	HIGH-level input current	V_{CLK} = 2.0 V	–	–	20	μA
Z_i	input impedance	f_{CLK} = 18 MHz	–	2	–	kΩ
C_i	input capacitance	f_{CLK} = 18 MHz	–	2	–	pF
INPUTS: CDSP1 AND CDSP2						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_{IL}	LOW-level input current	V_{IL} = 0.6 V	–	–100	–	μA
I_{IH}	HIGH-level input current	V_{IH} = 2.2 V	–	0	–	μA
INPUTS: SEN, STDBY, CLPCDS, CLPOPB, PBK AND CLPADC						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	V_{CCD}	V
I_i	input current		–2	–	+2	μA
INPUTS: SEN, SDATA AND SCLK (see Fig.14)						
t_{su1}	SEN set-up time compared to SCLK rising edge		–	4	–	ns
t_{su2}	SDATA set-up time compared to SCLK rising edge		–	4	–	ns
t_{su3}	SEN set-up time compared to SCLK falling edge		–	4	–	ns
t_{hd3}	SEN hold time compared to SCLK rising edge		–	4	–	ns
t_{hd4}	SDATA hold time compared to SCLK rising edge		–	4	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling; CDS						
$V_{i(CDS)(p-p)}$	CDS input amplitude (peak-to-peak value)		–	400	1200	mV
$I_{STGE,IN1,IN2}$	input current pins 19, 46 and 47		–2	–	+2	μA
$t_{CDS(min)}$	CDS control pulses minimum active time (HIGH for TDA8786, LOW for TDA8786A)	$f_{i(CDS1,2)} = f_{CLK(pix)}$ $V_{i(CDS)(p-p)}$ = 1200 mV black-to-white transition in one pixel (±1 LSB typ.)	12	–	–	ns
t_{hd1}	hold time IN1 compared to control pulse CDSP1	see Fig.15	–	1	–	ns
t_{hd2}	hold time of IN2 compared to control pulse CDSP2	see Fig.15	–	–0.5	–	ns
Amplifier outputs						
G_{AMPOUT}	output amplifier gain		–	6	–	dB
Z_{AMPOUT}	output amplifier impedance		–	300	–	Ω
$V_{AMPOUT(p-p)}$	output amplifier dynamic voltage level (peak-to-peak value)		–	2.4	–	V
$V_{AMPOUT(bl)}$	output amplifier black level voltage		–	1.1	–	V
$V_{AGCOUT(p-p)}$	AGC output amplifier dynamic voltage level (peak-to-peak value)		–	1800	–	mV
V_{AGCOUT}	AGC output amplifier black level voltage		–	1.1	–	V
Z_{AGCOUT}	AGC output amplifier output impedance	at 10 kHz	–	5	–	Ω
I_{AGCOUT}	AGC output static drive current	static	–	–	1	mA
$V_{OPB(p-p)}$	optical black clamp and blanking block output dynamic voltage (peak-to-peak value)		–	1.8	–	V
V_{OPB}	optical black clamp and blanking block output black level voltage		–	1.4	–	V
Z_{OPB}	optical black clamp and blanking block output impedance	at 10 kHz	–	–	5	Ω
I_{OPB}	OPB output current drive	static	–	–	1	mA
I_{PBIN}	input current pin 8		–2	–	+2	μA
$G_{AGC(min)}$	minimum gain of AGC circuit	AGC DAC input code = 00 (9-bit control)	–	3.5	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$G_{AGC(max)}$	maximum gain of AGC circuit	AGC DAC input code = ≥319 (9-bit control)	–	33.5	–	dB
V_{AGCOUT}	AGC output amplifier black level voltage		–	1.1	–	V
$V_{inflex(p-p)}$	voltage at soft clipper inflexion point (peak-to-peak value)	soft clipper 4-bit control DAC input code = 00	–	40% $V_{AGCOUT(p-p)}$	–	V
		soft clipper 4-bit control DAC input code = 15	–	100% $V_{AGCOUT(p-p)}$	–	V
CR_{sc}	soft clipper compression ratio	$V_{i(sc)} < V_{inflex}$	–	1.0	–	
		$V_{i(sc)} > V_{inflex}$	–	0.66	–	
CLAMPS						
g_{mADC}	ADC clamps transconductance	at clamp level	–	60	–	mS
g_{mPBK}	PBK clamp transconductance	at clamp level	–	60	–	mS
g_{mCDS}	CDS clamps transconductance	at clamp level	–	5.5	–	mS
$V_{PBIN(clamp)}$	clamp voltage at PBIN input		–	1.4	–	V
Analog-to-Digital Converter; ADC						
$f_{CLK(max)}$	maximum clock frequency		18	–	–	MHz
t_{CPH}	clock pulse width HIGH		15	–	–	ns
t_{CPL}	clock pulse width LOW		15	–	–	ns
SR_{CLK}	clock input slew rate (rising and falling edge)	10 to 90%	0.5	–	–	V/ns
$V_{i(ADC)(p-p)}$	ADC input voltage level (peak-to-peak value)		–	1.8	–	V
V_{RB}	ADC reference voltage output code 0		–	1.4	–	V
V_{RT}	ADC reference voltage output code 1023		–	3.2	–	V
I_{ADCIN}	input current pin 10		–2	–	+2	μA
ILE	integral linearity error	f_{CLK} = 18 MHz; ramp input	–	±1.0	±2.0	LSB
DLE	differential linearity error	f_{CLK} = 18 MHz; ramp input	–	±0.4	±0.75	LSB
$t_{d(s)}$	sampling delay time		–	–	5	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Total chain timing (CDS + ADC + SOFT CLIPPER + PRE BLANKING + ADC)						
t_d	time delay between CDSP1 and CLK	50% at rising edges of CLK and CDSP1: transition full-scale code 0 to code 1023; $V_{i(CDS)(p-p)}$ = 1200 mV	–	40	–	ns
$N_{(rms)}$	noise (RMS value)	gain = 3.5 dB	–	0.5	–	LSB
Digital-to-Analog Converters (OFDOUT DAC)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)		–	1.4	–	V
$V_{OFDOUT(0)}$	DC output voltage for code 0		–	2.0	–	V
$V_{OFDOUT(255)}$	DC output voltage for code 255		–	3.4	–	V
Z_{OFDOUT}	additional 8-bit control DAC (OFD) output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output current drive	static	–	–	50	μA
ADC clamp control DAC (see Fig.5)						
$V_{DACOUT(p-p)}$	ADC clamp 10-bit control DAC output voltage (peak-to-peak value)		–	0.9	–	V
V_{DACOUT}	DC output voltage	code 0	–	1.4	–	V
		code 1023	–	2.3	–	V
Z_{DACOUT}	ADC clamp control DAC output impedance		–	–	250	Ω
I_{DACOUT}	DAC output current drive	static	–	–	50	μA
OFE_{LOOP}	maximum offset error of DAC + ADC clamp loop	code 0	–	± 5	–	LSB
		code 1023	–	± 5	–	LSB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs (f_{CLK} = 18 MHz; C_L = 20 pF)						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
I_{OZ}	output current in 3-state mode	0.5 V < V_o < V_{CCO}	–20	–	+20	μA
$t_{o(h)}$	output hold time		5	–	–	ns
$t_{o(d)}$	output delay	C_i = 20 pF; V_{CCO} = 4.75 V	–	12	15	ns
		C_i = 20 pF; V_{CCO} = 3.15 V	–	17	20	ns
		C_i = 20 pF; V_{CCO} = 2.7 V	–	21	24	ns
Serial interface						
$f_{SCLK(max)}$	maximum frequency of serial interface		5	–	–	MHz

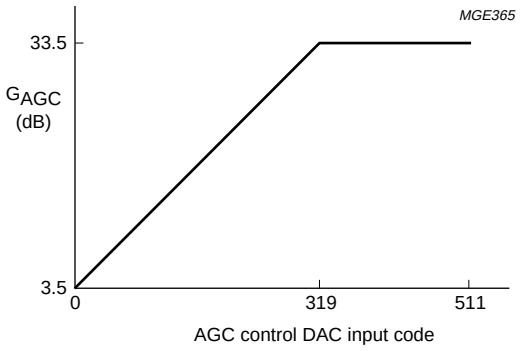
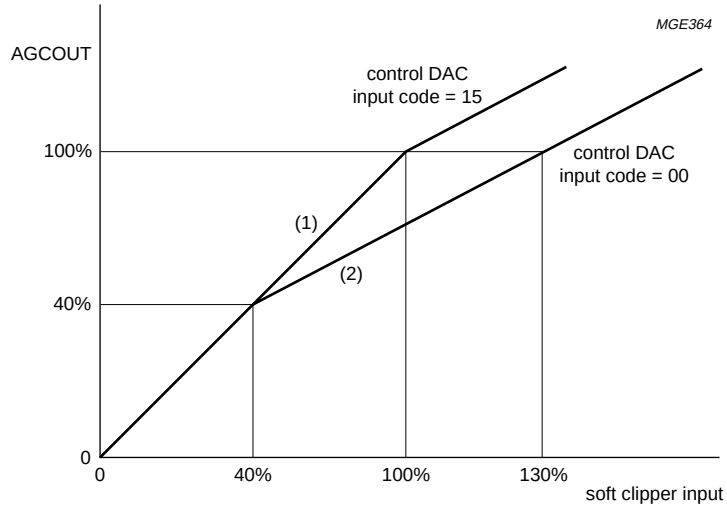


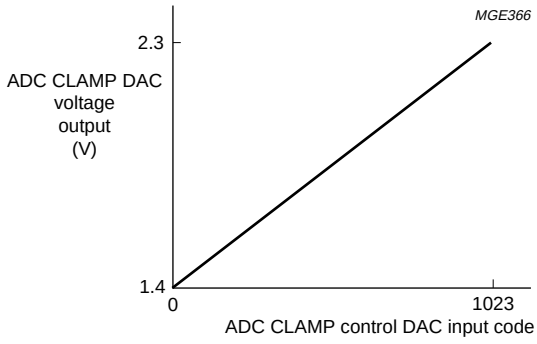
Fig.3 AGC gain as a function of DAC input code.



(1) $\frac{V_o}{V_i} = 1$

(2) $\frac{V_o}{V_i} = 0.66$

Fig.4 Soft clipper output voltage as a function of soft clipper input voltage.



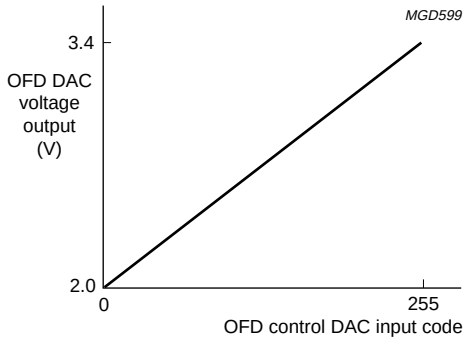


Fig.5 DAC voltage output as a function of DAC input code.

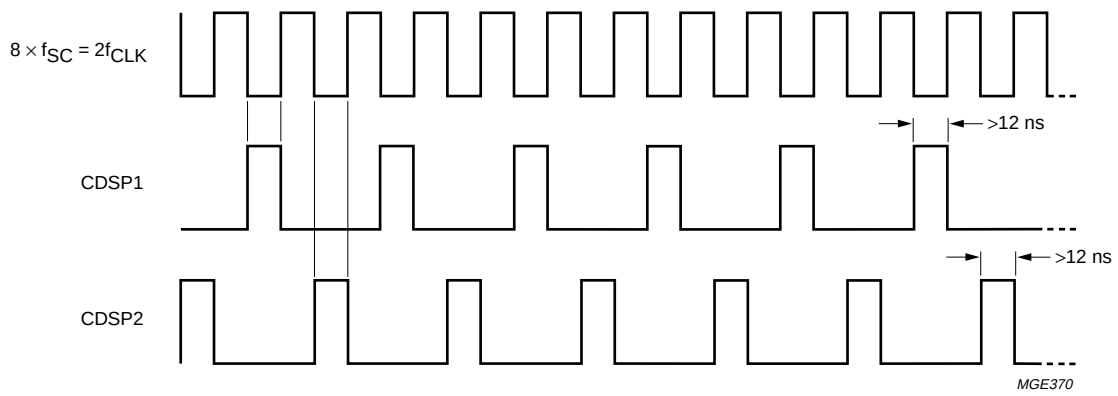


Fig.6 CCD high band control signal timing (TDA8786).

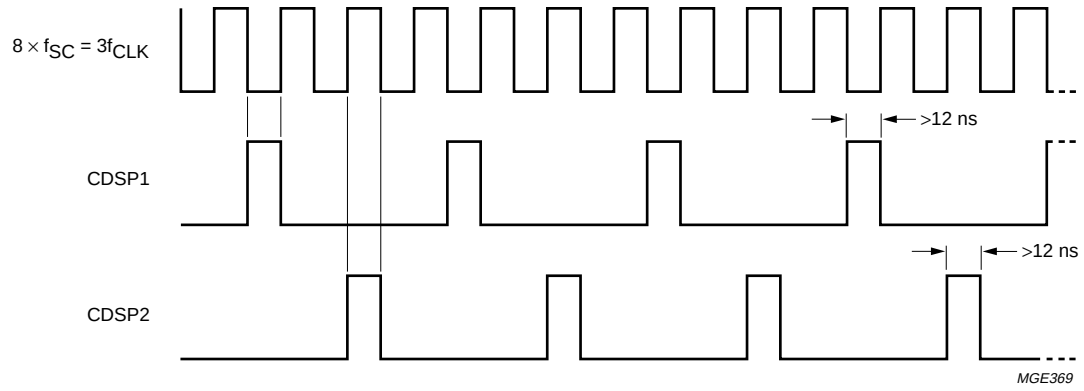


Fig.7 CCD normal band control signal timing (TDA8786).

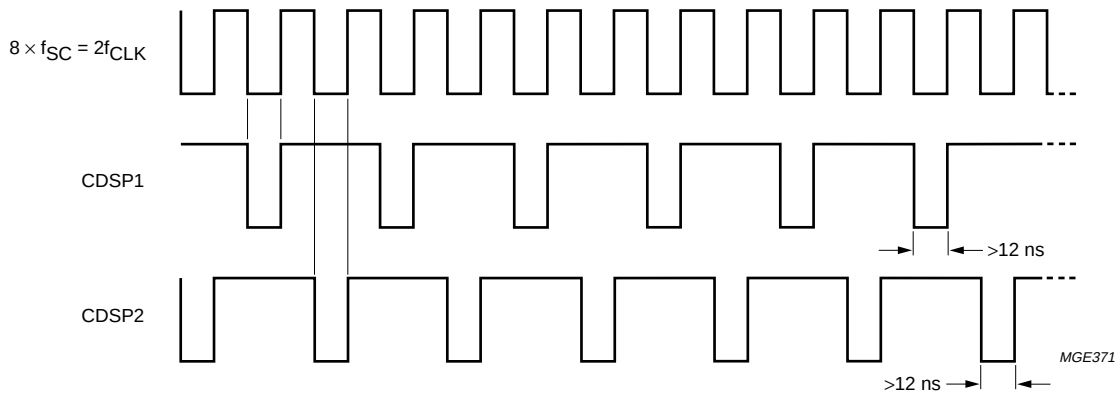


Fig.8 CCD high band control signal timing (TDA8786A).

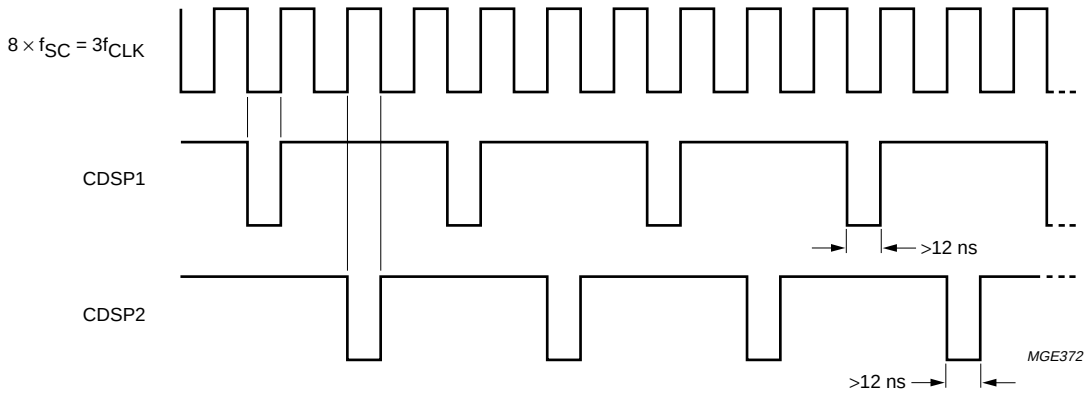


Fig.9 CCD normal band control signal timing (TDA8786A).

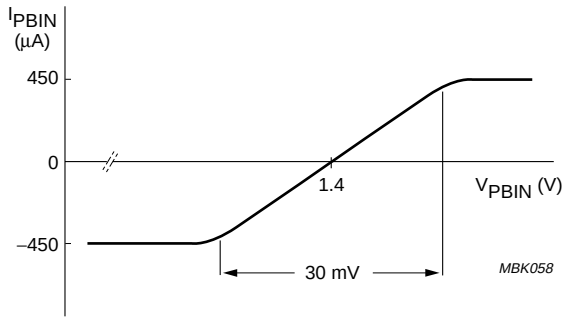


Fig.10 Typical PBK clamp current.

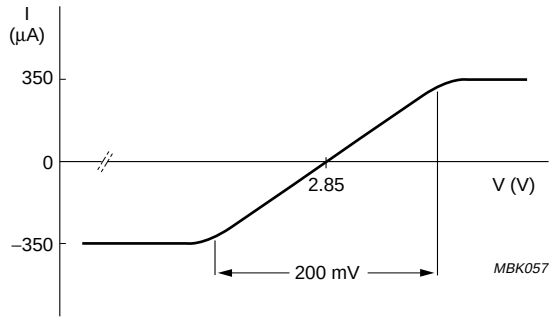


Fig.11 Typical clamp currents for pins IN1, IN2 and STGE.

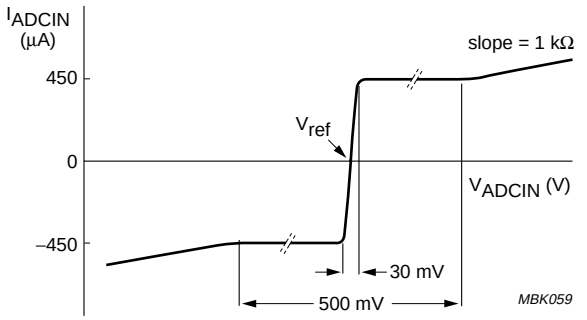


Fig.12 Typical ADC clamp current.

ADC clamping

When pin CLPADC is HIGH (TDA8786) (LOW for TDA8786A), the ADC input is clamped to voltage level V_{ref}. V_{ref} should normally be connected to V_{RB} (ADC reference voltage code 0) or to DACOUT (10-bit DAC output). The DAC is controlled via the serial interface, its output covers the lower half of the ADC input range.

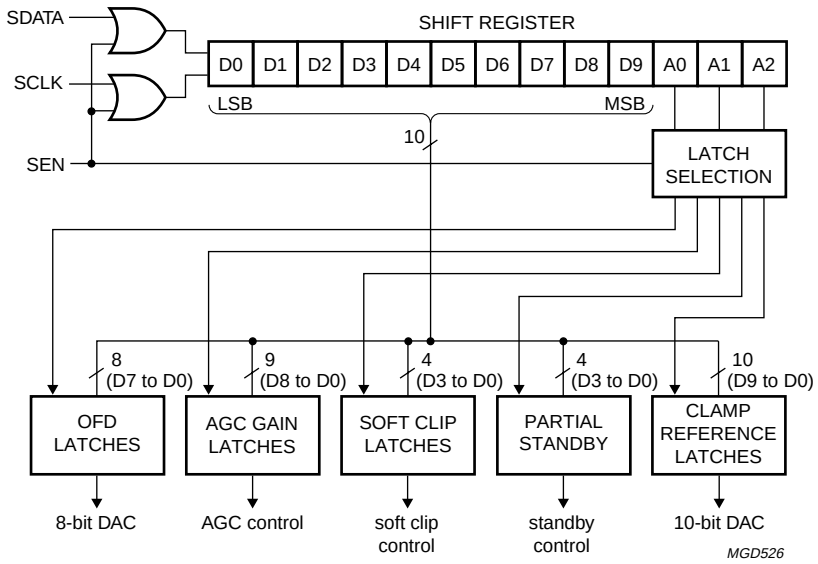
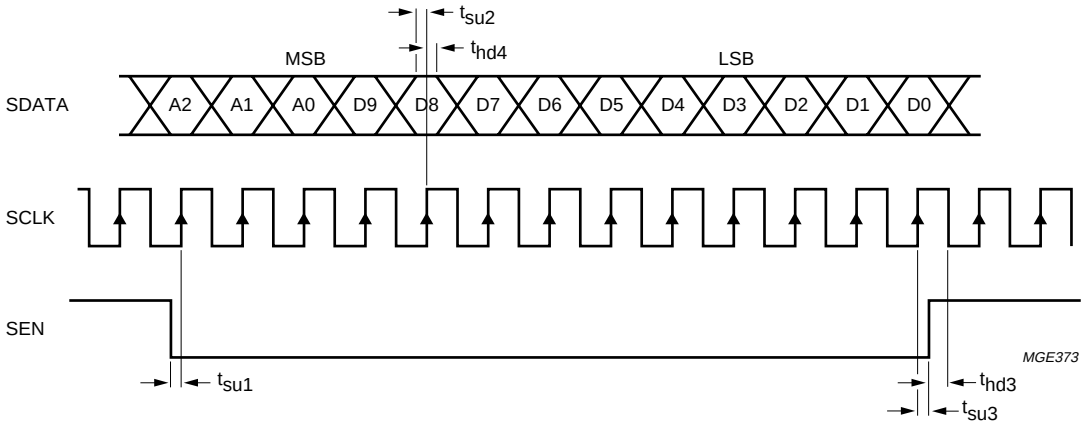


Fig.13 Serial interface block diagram.



t_{su} = 4 ns (min.); $t_{hd3} = t_{hd4}$ = 4 ns (min.).

Fig.14 Loading sequence of control DACs input data via the serial interface.

Table 1 Serial interface programming (see note 1)

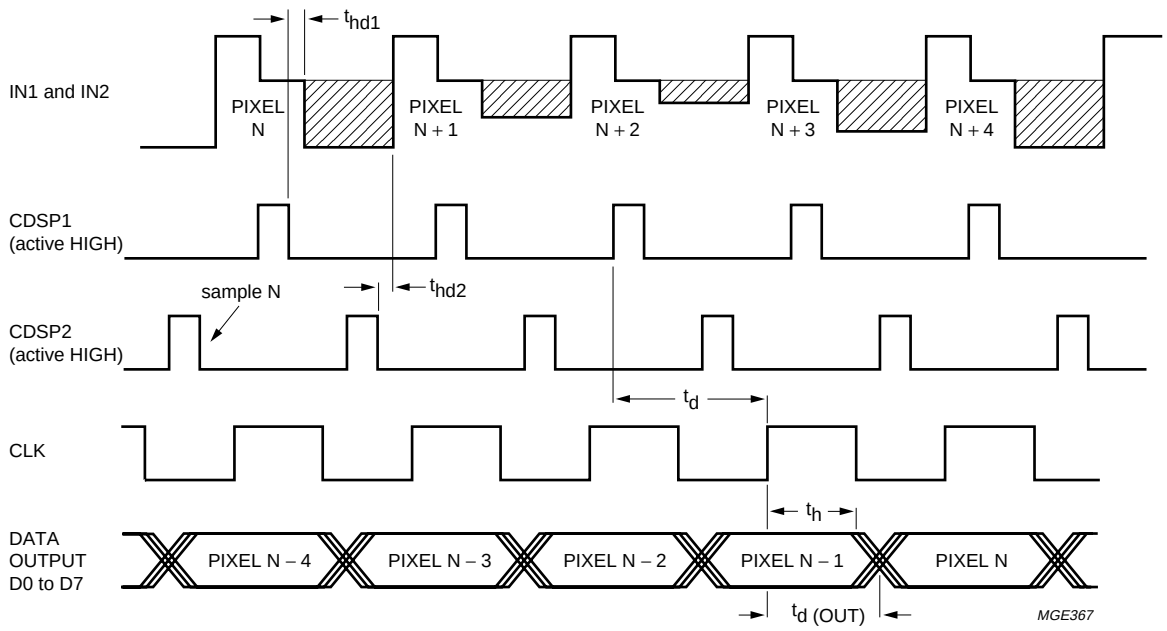
ADDRESS BITS			DATA BITS D9 to D0
A2	**A1**	**A0**	
0	0	0	OFDOUT output control (D7 to D0).
0	0	1	Soft clipper control. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0.
0	1	0	AGC gain control (D8 to D0).
0	1	1	Partial standby controls for power consumption optimization. Only the 4 LSBs (D3 to D0) are used. Bits D9 to D4 should be set to logic 0: D0 = 1: CDS + AGC + soft clipper block in standby; $I_{CCA} + I_{CCD}$ = 48 mA D1 = 1: optical black clamp + blanking block in standby; $I_{CCA} + I_{CCD}$ = 92 mA D2 = 1: OFD DAC in standby; $I_{CCA} + I_{CCD}$ = 98 mA D3 = 1: 6 dB amplifier (output on AMPOUT pin) in standby; $I_{CCA} + I_{CCD}$ = 98.5 mA.
1	0	0	Clamp reference DAC (D9 to D0).

Note

1. At the end of each programming sequence (usually during the video vertical blanking), the soft clipper register must be reloaded (for example if the soft clipper is not used, code 15 must be entered in the soft clipper register at the end of each TDA8786(A) programming sequence).

Table 2 Standby selection

STDBY	D9 to D0	$I_{CCA} + I_{CCD}$
1	LOW	4 mA (typ.)
0	active	99 mA (typ.)



The hatched areas represent active video.

Fig.15 Pixel frequency timing diagram.

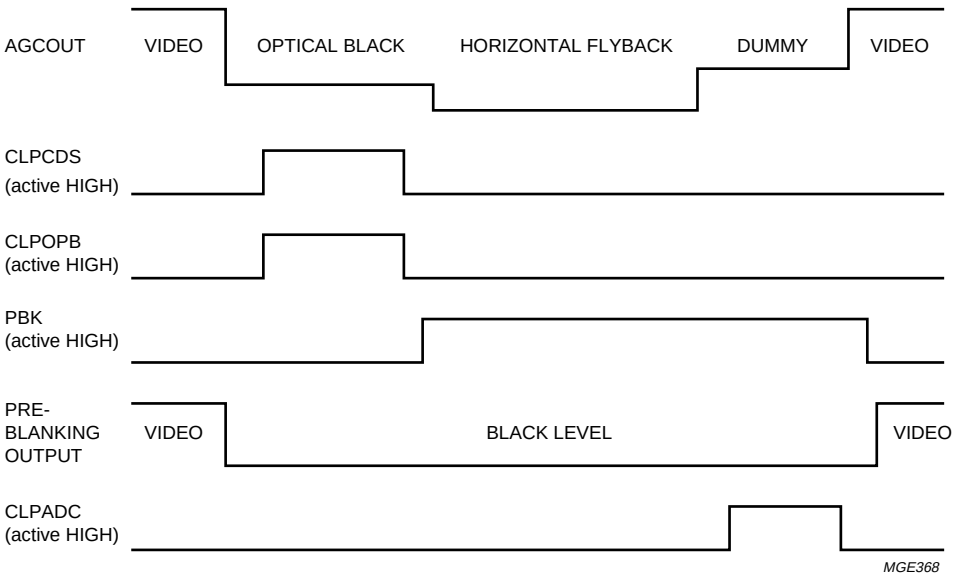


Fig.16 Line frequency timing diagram.

APPLICATION INFORMATION

TDA8786 and SAA8110 can be used with Sharp CCDs. TDA8786A and SAA8110 can be used with Sony CCDs. Table 3 gives as an example some references of ICs which may be used with Philips TDA8786(A)/SAA8110. This overview is not restrictive, both devices are compatible with other CCD/V-driver/PPG combinations including the more recent ones.

Table 3 Possible components for the application of Figs 17 and 18

CCD TYPE	COMPONENT TYPE	NTSC		PAL	
		MEDIUM RESOLUTION	HIGH RESOLUTION	MEDIUM RESOLUTION	HIGH RESOLUTION
Sony CCDs	CCD	LZ2313H5	LZ2353A	LZ2323H5	LZ2363
	V-driver	LR36683N			
	timing generator	LZ95G55	LZ95G71	LZ95G55	LZ95G71
Sharp CCDs	CCD	ICX056AK	ICX068AK	ICX057AK	ICXo69AK
	V-driver	CXD1250MN, CXD1267N			
	timing generator	CXD1257AR	CXD1265R	CXD1257AR	CXD1265R

Notes to the application diagram

1. In the configuration of Figs 17 and 18, the microcontroller reads and writes data from/to the DSP using the SNERT-bus (UART mode 0). Optional external control is available via the I^2C-bus.
2. Free I/O pins of the microcontroller can be used to control PGG, or for other purposes.
3. 83Cxxx processing is synchronized by VD interruption. Depending on VD polarity, it can be necessary to invert VD.
4. A customized 83Cxxx is available for this application. Please contact your nearest Philips sales office.

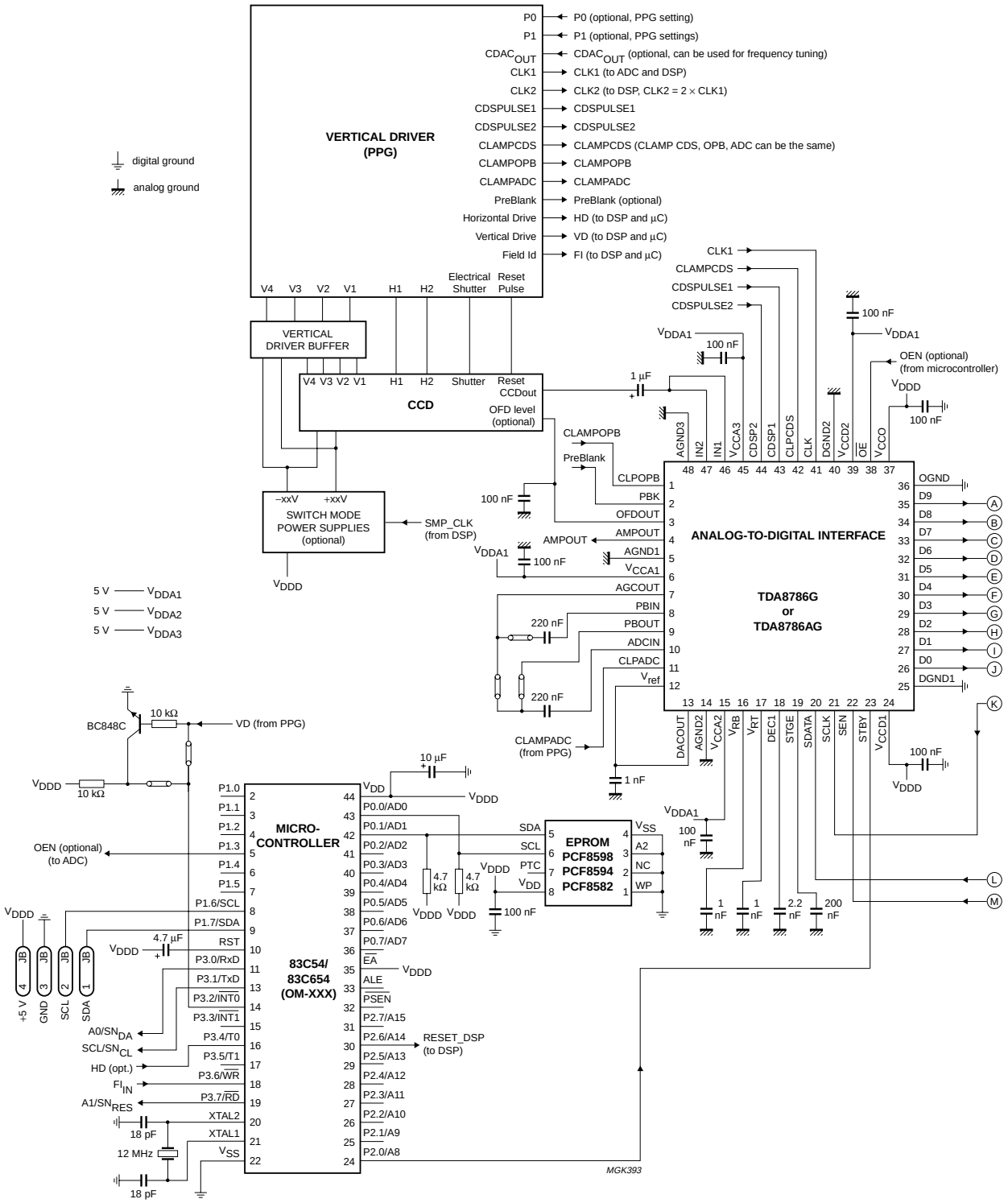
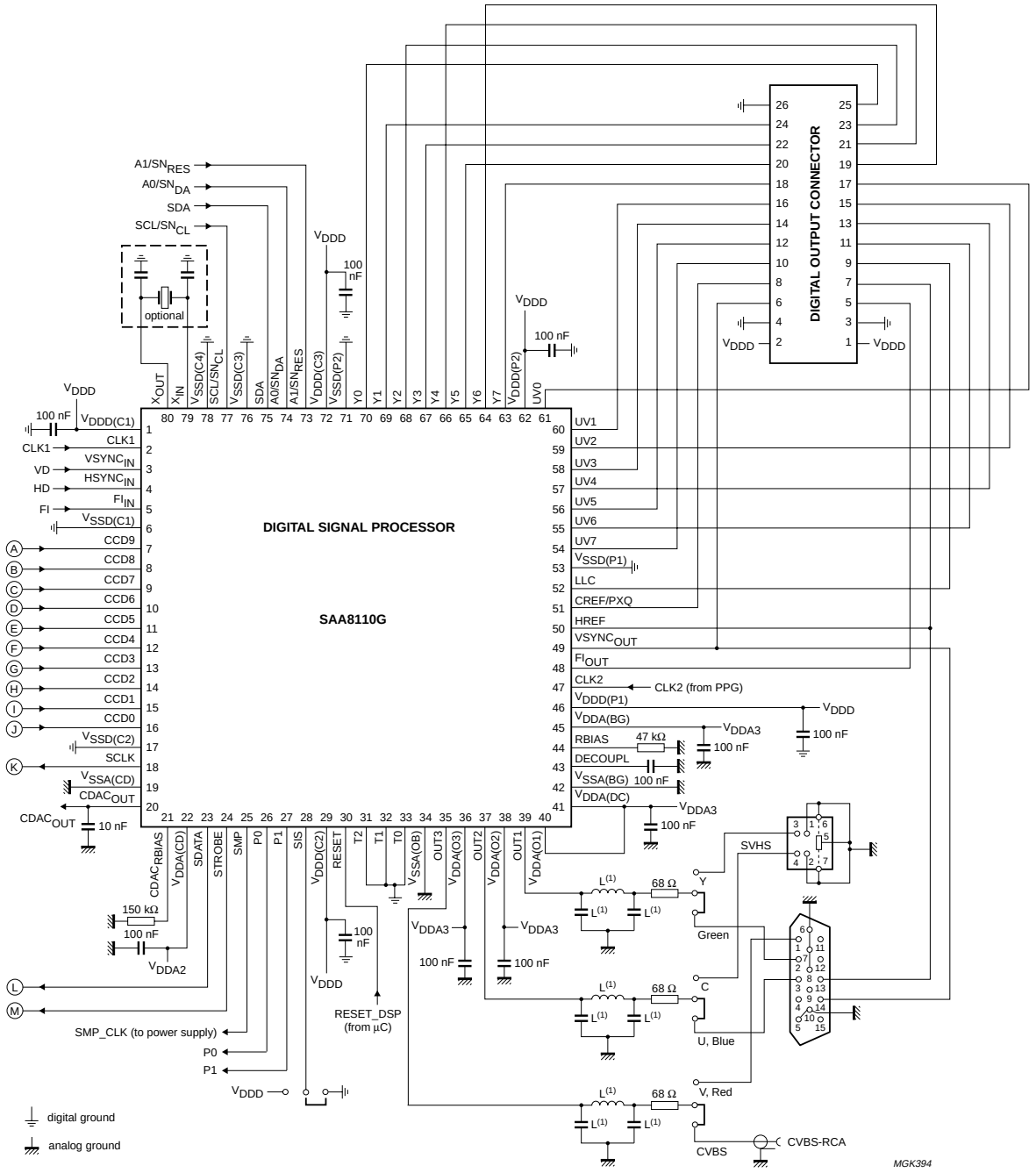


Fig.17 SAA8110G system configuration for camera application (continued in Fig.18).

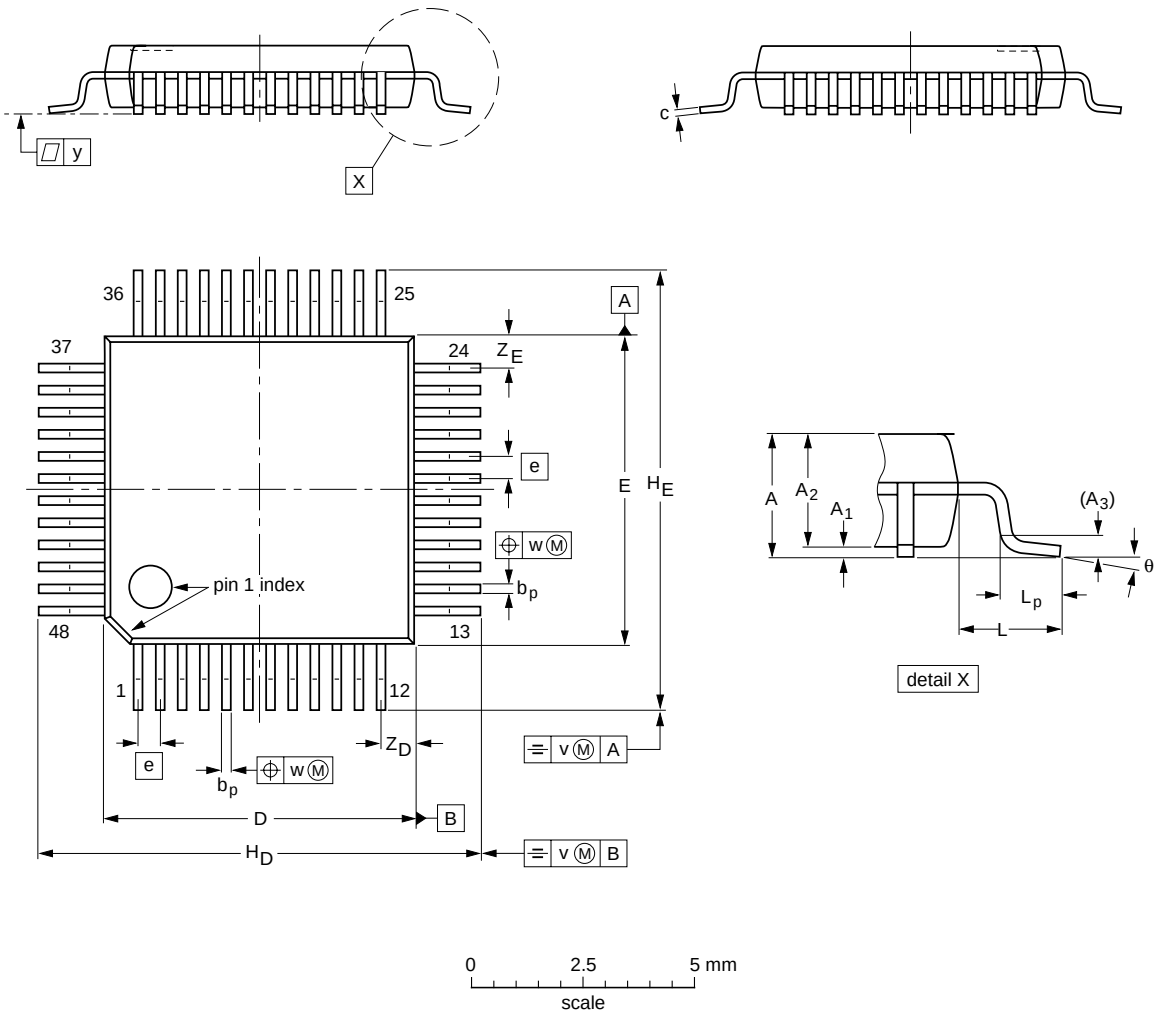


(1) Values depend on DSP output configuration.

Fig.18 SAA8110G system configuration for camera application (continued from Fig.17).

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010,
Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p,
P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 547047/1200/03/pp28 Date of release: 1997 Nov 17 Document order number: 9397 750 02926

Let's make things better.

Philips Semiconductors

PHILIPS